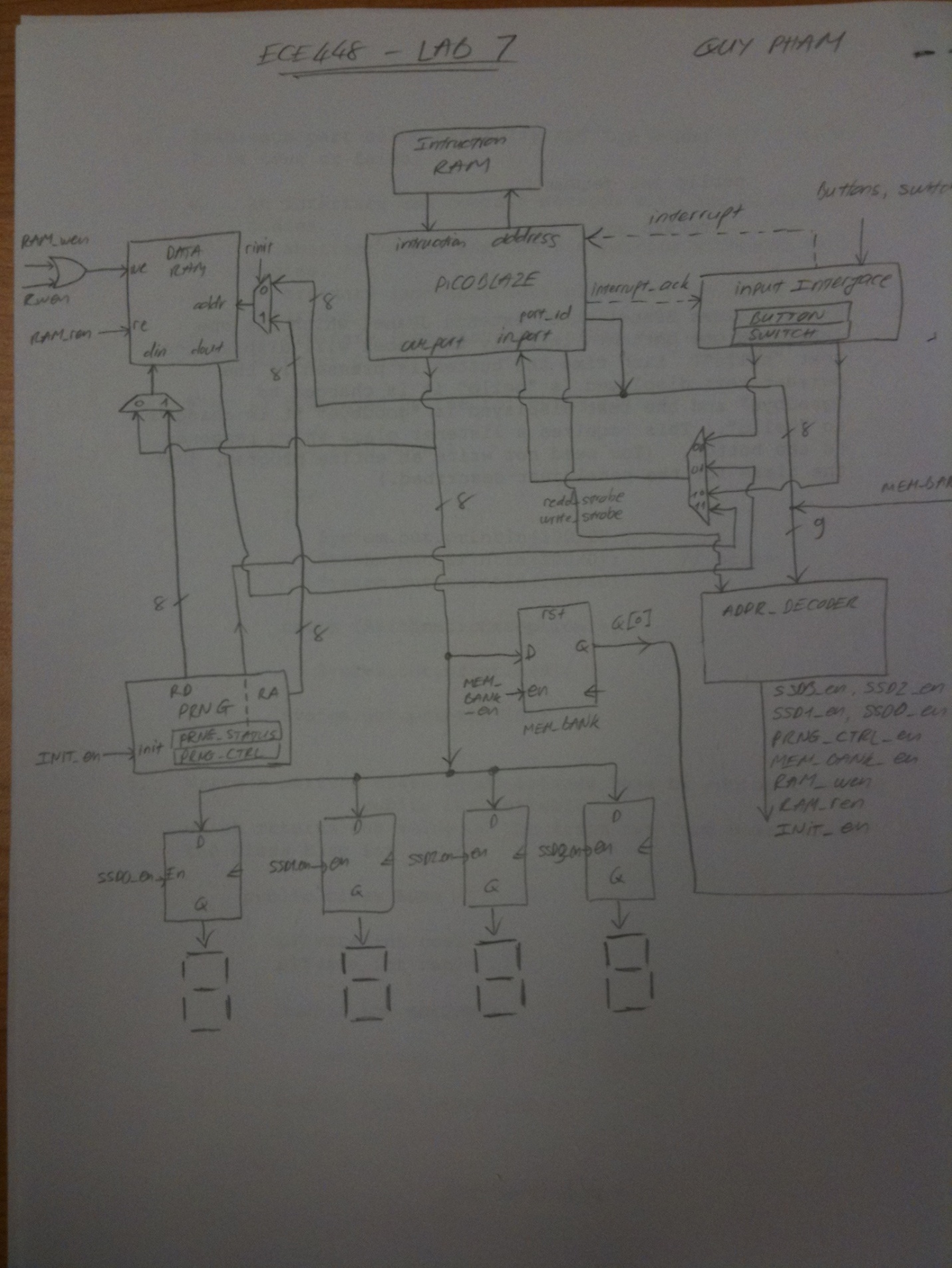
**Lab 7 – Report**

**Block Diagram**



Design Summary

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Number of errors: 0

Number of warnings: 65

Logic Utilization:

Number of Slice Flip Flops: 207 out of 1,920 10%

Number of 4 input LUTs: 354 out of 1,920 18%

Logic Distribution:

Number of occupied Slices: 272 out of 960 28%

Number of Slices containing only related logic: 272 out of 272 100%

Number of Slices containing unrelated logic: 0 out of 272 0%

Total Number of 4 input LUTs: 440 out of 1,920 22%

Number used as logic: 286

Number used as a route-thru: 86

Number used for Dual Port RAMs: 16

(Two LUTs used per Dual Port RAM)

Number used for 32x1 RAMs: 52

(Two LUTs used per 32x1 RAM)

The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

Number of bonded IOBs: 33 out of 83 39%

Number of RAMB16s: 2 out of 4 50%

Number of BUFGMUXs: 2 out of 24 8%

Number of DCMs: 1 out of 2 50%

Timing Summary:

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Speed Grade: -4

Minimum period: 12.288ns (Maximum Frequency: 81.380MHz)

Minimum input arrival time before clock: 8.372ns

Maximum output required time after clock: 7.670ns

Maximum combinational path delay: No path found